Trapping hot quasi-particles in a high-power electronic cooler

H. Q. Nguyen

Low Temperature Laboratory (OVLL), Aalto University School of Science, P.O. Box 13500, 00076 Aalto, Finland

E-mail: hung@ltl.tkk.fi

T. Aref

Low Temperature Laboratory (OVLL), Aalto University School of Science, P.O. Box 13500, 00076 Aalto, Finland

E-mail: thomasaref@gmail.com

V. J. Kauppila

Low Temperature Laboratory (OVLL), Aalto University School of Science, P.O. Box 13500, 00076 Aalto, Finland

E-mail: ville.kauppila@aalto.fi

M. Meschke

Low Temperature Laboratory (OVLL), Aalto University School of Science, P.O. Box 13500, 00076 Aalto, Finland

E-mail: meschke@boojum.hut.fi

C. B. Winkelmann

Institut Néel, CNRS, Université Joseph Fourier and Grenoble INP, 25 avenue des Martyrs, 38042 Grenoble, France

E-mail: clemens.winkelmann@grenoble.cnrs.fr

H. Courtois

Institut Néel, CNRS, Université Joseph Fourier and Grenoble INP, 25 avenue des Martyrs, 38042 Grenoble, France

E-mail: herve.courtois@grenoble.cnrs.fr

J. P. Pekola

Low Temperature Laboratory (OVLL), Aalto University School of Science, P.O. Box 13500, 00076 Aalto, Finland

E-mail: jukka.pekola@aalto.fi

Abstract. The performance of hybrid superconducting electronic coolers is usually limited by the accumulation of hot quasi-particles in the superconducting leads. This issue is all the more stringent in large-scale and high-power devices, as required by applications. Introducing a metallic drain connected to the superconducting electrodes via a fine-tuned tunnel barrier, we efficiently remove quasi-particles and obtain electronic cooling from 300 mK down to 130 mK with a 400 pW cooling power. A simple thermal model accounts for the experimental observations.

1. Introduction

On-chip solid-state refrigeration has long been sought for various applications in the sub-kelvin temperature regime, such as cooling astronomical detectors [1, 2, 3]. In a Normal metal - Insulator - Superconductor (NIS) junction [4, 5, 6], the superconductor density of states gap makes that only high-energy electrons are allowed to tunnel out of the normal metal or, depending on the bias, low-energy ones to tunnel in, so that the electronic bath as a whole is cooled. In SINIS devices based on aluminum, the electronic temperature can drop from 300 mK down to below 100 mK at the optimum bias point. While this level of performance has been demonstrated in micron-scale devices [7, 8] with a cooling power in the picoWatt range, a difficulty arises in devices with large-area junctions needed for a sizable cooling power approaching the nanoWatt range. For instance, a high-power refrigerator has been shown to cool an external object from 290 mK to about 250 mK [9]. One of the main limitation to NIS coolers' full performance is the presence of non-equilibrium quasi-particles arising from the high current running through the device. The low quasi-particle relaxation rate and thermal conductivity in a superconductor bound these hot particles in the vicinity of the junction and lead to severe overheating in the superconducting electrodes.

There are several methods for reducing the accumulation of quasi-particles in a superconductor. For example a small magnetic field [10] can be used to introduce vortices that trap quasi-particles. This approach is however not applicable to electronic coolers with large-area junctions since a vortex also reduces the cooling performance if it resides within a junction. The most common method is to use a normal metal coupled to the superconductor as a quasi-particle trap: quasi-particles migrate to the normal metal and relax their energy there through electron-electron and electron-phonon interaction. In the typical case of a fabrication process based on angle evaporation, a quasi-particle trap is a structure mirroring the superconducting electrode, sitting on a side of the cooling junction and featuring the same oxide barrier layer. The trapping efficiency is usually moderate, but can be improved in two ways: the normal metal can be put in direct contact with the superconductor, as out-of-equilibrium quasi-particles would diffuse more efficiently to the trap [11], or the trap can be closer to the junction [12, 13]. In both cases, it is important to prevent inverse proximity effect in the superconductor, which smears locally the superconductor density of states and degrades cooling efficiency. The existence of an optimum transparency for the interface between the trap and the superconducting lead is therefore expected, which remains to be investigated [14].

In this paper, we present an effective method to evacuate quasi-particles in a SINIS cooler, which we call a quasi-particle drain. It is a layer of normal metal located at a fraction of superconducting coherence length away from the junction and separated by a thin insulating layer to stop the inverse proximity effect. We compare the cooling performance when varying the quasi-particle drain barrier transparency over a wide range. The efficiency of the quasi-particle drain is demonstrated through the electronic cooling from 300 to 130 mK at a 400 pW cooling power in an optimized device. A

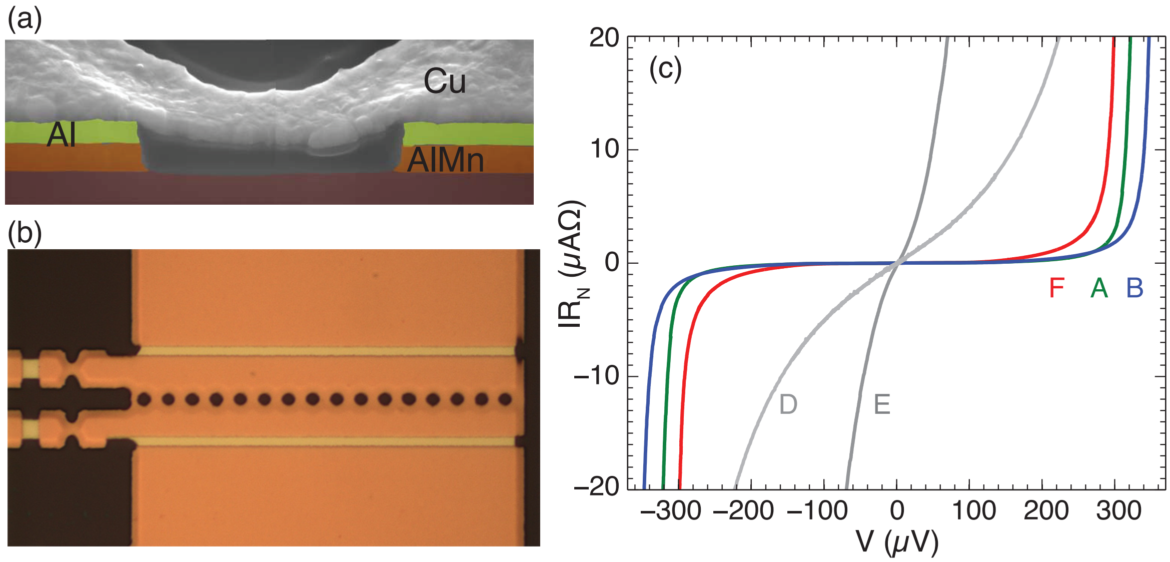

Figure 1. (a) False-colored scanning electron side micrograph of a SINIS cooler showing from top to bottom: 100 nm of Cu (normal metal N), 200 nm of Al (superconductor S), and 200 nm of AlMn (quasi-particle drain) with AlOx insulating layers in-between (not visible). (b) Top view of the cooler showing the array of holes connecting the two NIS junctions. Each hole has a diameter of 2 μm. Cu appears as orange and the Al/AlMn bilayer as yellow. (c) Current-voltage characteristics at a 50 mK temperature of samples A, B, D, E and F, with different tunnel barrier thicknesses between the quasi-particle drain and the superconducting leads, see Table 1.

simple thermal model captures the effect of the drain reasonably well.

2. Fabrication and measurement methods

We use the fabrication process described in Ref. [15], in which a SINIS cooler is obtained by photo-lithography and chemical etch of a NIS multilayer. Here, we add a normal metal layer at the bottom, which is used as a quasi-particle drain. Figure 1a false-colored scanning electron micrograph shows a side view of a typical SINIS cooler, obtained by cutting it with a focused ion beam. From top to bottom, the 100 nm-thick Cu normal metal layer to be cooled is suspended between two 200 nm-thick Al superconducting electrodes. The latter layers rest on a quasi-particle drain made of a 200 nm layer of AlMn deposited on a Si wafer. We choose AlMn [16, 17] as a quasi-particle drain normal material because it acts chemically as Al in terms of oxidation and etch. The layers are separated by two aluminum oxide barriers, which we name the drain barrier between the AlMn and Al layers and the cooler barrier between the Al and Cu layers. Sample parameters are given in Table 1.

Figure 1b is an optical micrograph showing a top view of the cooler. A trench in the Al and AlMn layers, created by chemical over-etch underneath the array of holes in the suspended Cu layer, separates the two NIS junctions. Each junction has an area of 70 ×

Table 1. SINIS cooler parameters. All coolers are made of layers of 100 nm of Cu, 200 nm of Al, and 200 nm of AlMn and have a junction size of 70×4 μm^2. As an exception, sample F has no AlMn layer as a quasi-particle drain and the thickness of Al is 400 nm. We indicate oxygen pressure and oxidation time used for the preparation of the AlMn/Al drain barrier and of the Al/Cu cooler barrier. R_N and 2Δ are the normal state resistance and twice the superconducting energy gap, respectively, obtained by fitting the IV characteristics to Eq. 1. "Color" refers to the figures throughout the paper.

Sample	Drain barrier (mbar, second)	Cooler barrier (mbar, second)	R_N (Ω)	2Δ (μeV)	Color
A	1.3, 10	1.3, 300	0.71	398	green
B	0.26, 10	1.3, 300	1.56	382	blue
C	0.18, 1	0.8, 180	0.55	370	purple
D	5×10^{-4}, 10	1.3, 300	1.01	228	gray
E	0	1.3, 180	1.31	180	gray
F	N/A	1, 300	0.83	390	red

4 μm^2 and is surrounded by two quasi-particle traps: a side trap made of Cu next to it, and a quasi-particle drain made of AlMn. Two additional small NIS junctions connected to the normal metal are used as a SINIS thermometer. Electron temperature is accessed by comparing the measured voltage drop under a small bias current (typically 10 nA) to a calibration against the cryostat temperature.

The current flowing through a NIS junction writes

$$I_{NIS} = \frac{1}{eR_N}\int dE(E-eV)n_S(E)[f_N(E-eV)-f_S(E)], \tag{1}$$

where n_S is the normalized superconductor density of states, R_N is the normal state junction resistance, and $f_{S,N}$ are the Fermi-Dirac energy distributions of electrons in S and N, respectively. If leakage is negligible, a low sub-gap current then means a low electronic temperature.

3. Experimental results and discussion

Figure 1c shows a current voltage characteristics (IV curve) of different samples measured with a standard current-biased 4-probe technique in a dilution cryostat, with a focus on the low-bias regime. The two innermost curves stand for samples E and F, which have no drain barrier and a very thin drain barrier, respectively. Superconductivity in the Al layers is then affected by a strong inverse proximity effect, which results in a depressed critical temperature and a low superconducting gap Δ so that $2\Delta = 180$ μeV and 228 μeV respectively.

As samples A, B, and C are fabricated using a higher oxidation pressure for the drain barrier, they have a typical value for 2Δ of about 350 μeV and a ratio of minimum conductance to normal-state conductance of about 10^{-4}, indicating that inverse proximity effect is weak. Samples A, B and C show a sharp characteristic, with

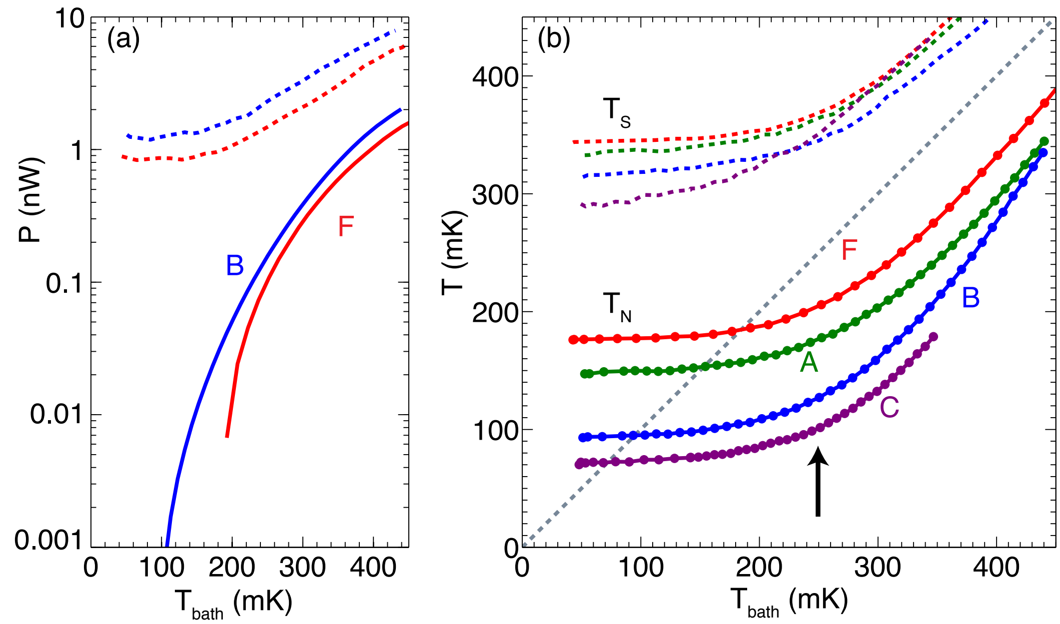

Figure 2. (a) Cooling power (solid lines) and input power (dashed line) of cooler B (blue) and F (red) as a function of the bath temperature. (b) Calculated electron temperature (dashed lines) of the superconductor and measured normal metal temperature (dots, connected by solid lines as a guide to the eye) at the optimum point for samples A, B, C and F. The dashed gray line is a one to one line, indicating the bath temperature. The arrow marks the bath temperature of 250mK, where sample C cools down to below 100 mK.

sample C (not shown) behaving almost identically to sample B. The sole difference between samples A and B is the drain barrier. Having a thinner barrier, sample B exhibits less current at a given sub gap bias, i.e. less overheating from quasi-particles in the superconductor. The drain barrier lets quasi-particles get efficiently trapped in the drain, while it stops the inverse proximity effect.

We estimate the cooling power from the electron-phonon coupling power in the normal metal volume:

$$\dot{Q}_{ep} = \Sigma^N \mathcal{V}(T_N^5 - T_{ph}^5), \tag{2}$$

where $\Sigma^N = 2 \times 10^9$ WK^{-5}m^{-3} in Cu [18], $\mathcal{V} = 83$ μm^3 is the island volume for all samples, T_N is the measured electron temperature and T_{ph} is the phonon temperature, both in the normal island. We assume here that $T_{ph} = T_{bath}$, which leads to an upper limit on the estimation of the cooling power. Figure 2 a displays the electron-phonon coupling power $\dot{Q}_{ep}$ (solid lines) and the total Joule power (dashed lines) $P_{IV} = I_{opt}V_{opt}$ measured at the optimum bias, i.e. the bias at which electronic cooling is maximum. The typical power scale for all our present coolers is in the nanoWatt range.

Figure 2 b presents the most important result of our work, namely the behavior of the normal island electronic temperature at optimum bias as a function of the bath temperature. All coolers perform the best at a bath temperature around 300 mK. At

lower temperatures, heating above the bath temperature arises from the sub-gap current. Having only the side trap and no quasi-particle drain, sample F shows a poor cooling from 300 mK down to only 230 mK. Carrying a quasi-particle drain, sample A cools to 200 mK. With a reduced drain barrier, sample B cools to 160 mK. In sample C, we obtain the best cooling by further reducing the drain and the cooler barriers: from 300 mK, sample C cools down to 132 mK with a 400 pW cooling power. Most importantly, from a bath temperature of 250 mK, sample C cools down to below 100 mK, see the arrow in Fig. 2b.

The electronic temperature of the superconducting electrodes can be accessed by balancing the normal metal electron-phonon coupling power (Eq. 2) with the NIS junction cooling power:

$$\dot{Q}_{NIS} = \frac{1}{e^2 R_N} \int dE (E - eV) n_S(E) [f_N(E - eV) - f_S(E)]. \tag{3}$$

Figure 2 b upper part (dashed lines) displays the electronic temperature of the superconductor T_S derived when assuming again $T_{ph} = T_{bath}$ in the normal metal. Although the latter assumption calls for further discussion, the trend remains that the superconductor gets significantly overheated.

4. Thermal model

In order to describe further the thermal transport in our devices, we consider a one-dimensional thermal model. The model geometry shown in figure 3a includes a normal metal island (N), superconducting leads (S), side traps (ST), and quasi-particle drains (D). The effect of the trap and the drain is described using the expression of the heat flow through a NIS junction. Although a non-equilibrium description of a biased NIS junction is possible [19, 20], we assume for simplicity a local thermal equilibrium in every part of the device. We also neglect inverse proximity effect in the superconductor, as can be justified by the sharpness of measured IVs. We obtain:

$$\begin{aligned}
\kappa_N \nabla^2 T_N \quad &= \mathcal{P}_{NIS}(V, T_S, T_N, R_N)/d_N - \mathcal{P}_{ep}^{N}(T_N)/d_N, \\
\nabla.(\kappa_S \nabla T_S) &= \mathcal{I}_{NIS}(V, T_S, T_N, R_N)V - \mathcal{P}_{NIS}(V, T_S, T_N, R_N)/d_S \\
&\quad - \mathcal{P}_{NIS}(0, T_S, T_D, R_D)/d_S, \\
\kappa_N \nabla^2 T_{ST} \quad &= \mathcal{P}_{NIS}(0, T_S, T_{ST}, R_N)/d_N - \mathcal{P}_{ep}^{ST}(T_{ST})/d_N, \\
\kappa_D \nabla^2 T_D \quad &= \mathcal{P}_{NIS}(0, T_S, T_D, R_D)/d_D - \mathcal{P}_{ep}^{D}(T_D)/d_D,
\end{aligned} \tag{4}$$

where $\mathcal{I}_{NIS}$, $\mathcal{P}_{NIS}$ and $\mathcal{P}_{ep}^{i}$ are the current I_{NIS}, the cooling power $\dot{Q}_{NIS}$ and the electron-phonon coupling power $\dot{Q}_{ep}$ calculated per unit area. T_i is the temperature, d_i is the thickness, Σ^i is the electron-phonon coupling term appearing in $\mathcal{P}_{ep}^{i}$ expression, and κ_i is the thermal conductivity in each element i. In the suspended region N1, the equation for T_N does not have the $\mathcal{P}_{NIS}$ term. In the side trap region, the equation for T_S does not have the $\mathcal{I}_{NIS}V$ term. Finally, the equation for T_D is ignored for sample F as it does not have a quasi-particle drain.

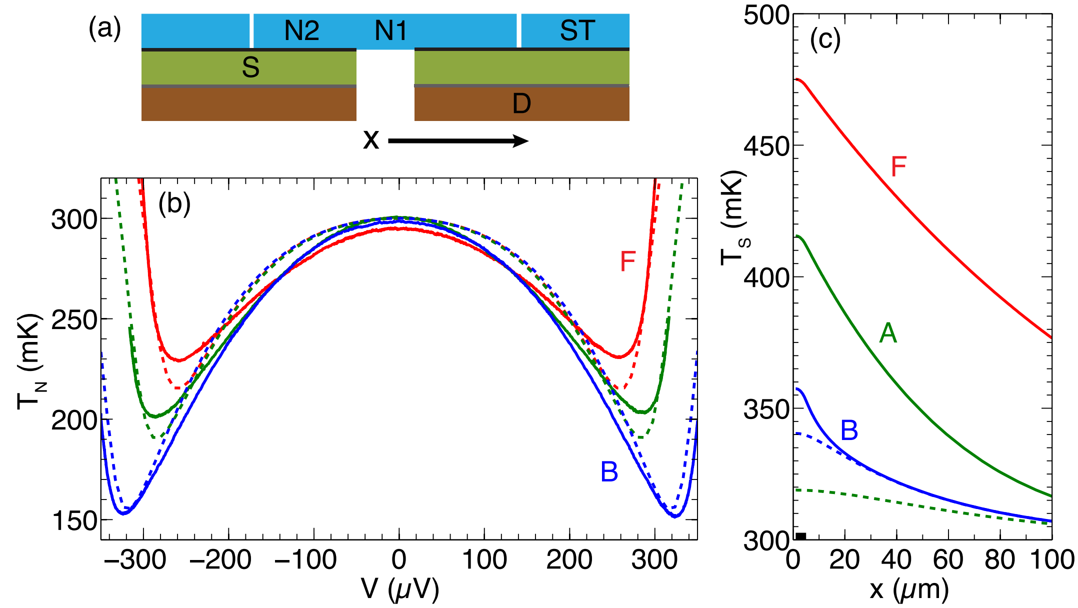

Figure 3. Finite element study of the heat transport in coolers A, B and F. (a) Geometry of the model: N1 is the suspended part of the normal island, N2 stands for the junction areas, S for the superconducting electrodes, ST for the side traps, and D for the quasi-particle drains. The layers are separated by tunnel barriers. (b) Electronic temperature drop as a function of bias at a 300 mK bath temperature, solid lines are measured data while dashed lines are calculated from the model. (c) Temperature of the superconductor S (solid lines) and of the quasi-particle drain D (dashed lines) as a function of the distance from the junction. The black bar indicates the junction location.

We solved the coupled differential equations numerically using COMSOL [21] with measured parameters from samples A, B, and F at 300 mK. We use the tabulated value for Cu and Al: $\kappa_N = 0.9$ WK^{-2}m^{-1} [6], $\kappa_D = 0.47\kappa_N$ [16], $\Sigma^D = 10^9$ WK^{-5}m^{-3} [17]. We take into account the exponential decay of κ_S with temperature [22]. For the cooler barrier, we use $R_N = 500\ \Omega\mu$m^2, close to the measured value for sample A (400 $\Omega\mu$m^2) and B (700 $\Omega\mu$m^2). As the drain barrier cannot be measured directly, we make a hypothesis $R_D = 500$ and 10 $\Omega\mu$m^2 for samples A and B respectively, in agreement with measured resistivities on samples with comparable oxidation parameters.

Figure 3b compares the modeling (dashed lines) with the experimental data (solid lines). The good match between the two confirms that our simple model captures the essential physics of the device despite its strong assumptions. Figure 3 c shows the calculated temperature profile in the superconductor (solid lines) and in the drain (dashed lines). It consistently shows that superconducting electrodes get overheated over a typical length scale of about 50 μm from the junction. Consistently with the electronic cooling amplitude observed, this overheating is less for samples A and B.

5. Conclusions

Our coolers can cool an electronic bath from 250 mK, the base temperature of a He^3 cryostat, down to below 100 mK, the working regime of a dilution cryostat. A quasiparticle drain is efficient in thermalizing NIS junctions. The related geometry does not impose any limit in making the junction larger, thus opening the possibility to obtain a cooling power well above the present level of 400 pW. The fabrication is low cost and involves only photolithography, the device is of high quality and robust. On this basis, we are developing a platform that integrates coolers and sensors on a single chip, which is of great potential for astrophysics and other low temperature applications.

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